REMARKS

Claims 1-30 are pending. Claim 14 was rejected because of an informality. Claim 14 has been amended to address the informality. Independent claims 1, 17, and 30 were rejected under 35 U.S.C. 103(a) as being unpatentable over Floman (USPN 2004/0199741) in view of Yip (USP 5,623,645).

Floman describes a memory controller. "The hardware unit can be realized in particular in the form of a chip which comprises only the memory control functionality or in addition some other functionalities, like a standard processor chip. In case the chip is realized as an ASIC, the memory controller enables typically only one of the functions of the ASIC, not the main function. In case the hardware unit is realized in form of a chip which has to co-operate with a main processor of an electronic device, for instance of a PC, there has to be some agreed interface between the processor and the chip." (Floman, Paragraph 22)

"The host 1 includes an ASIC 2 as an embodiment of the hardware unit according to the invention. The ASIC 2 comprises a software and hardware based memory controller, a bus and interface pins 3-6. The memory controller and the interface pins 3-6 are connected within the ASIC 2 to the bus. A first and a second group 3, 4 of y interface pins each are destined for a data exchange with one or more mass memory components, while a third and a fourth group 5, 6 of x interface pins each are destined for an exchange of control signals with one or more mass memory components. The first and second group 3, 4 of interface pins can each comprise e.g. y=4 pins, while the third and fourth group 5, 6 of interface pins can each comprise e.g. x=2 pins, thus there may be e.g. a total of 12 interface pins. Each mass memory component connected to the ASIC 2 is connected to one group 5, 6 of interface pins destined for an exchange of control signals and to at least one group 3, 4 of interface pins destined for an exchange of data." (Floman, Paragraph 32) Floman does not teach or suggest a programmable chip including a processor and a memory controller. Floman also does not teach or suggest "wherein the memory controller is user configurable to either use separate sets of I/O lines for accessing off-chip tristate devices or to share one or more I/O lines for accessing off-chip tristate devices."

The Examiner argues that Yip in Figure 3 describes a system on a chip that includes both a memory controller and a processor. Yip describes "FIG. 3 is a block diagram of

computer system 300 utilizing aspects of the present invention. Computer system 300 comprises a host processor system chip set which includes host processor 302, cache memory 304, bridge/memory controller 322, and dynamic random access memory 316. Host processor 302 may be any one of a number of commercially available microprocessors such as those marketed by Intel™ (Santa Clara, Calif.) and Motorola™ (Schaumburg, Ill.). PCI bus 334 couples bridge-memory controller 322 to a number of external devices such as local area network controller 324, hard disk controller 326, audio controller 318, video graphics array 330, and other expansion bus interfaces 328. Video graphics array 330 may drive display device 332 such as a monitor or a liquid crystal display device." (Column 4, Lines 15-29)

"Bridge/memory controller 322 is used to directly access any external device coupled to PCI bus 334. Generally, such external devices are mapped in memory or I/O address spaces. Bridge/memory controller 322 also performs data buffering/posting and PCI bus central functions (e.g., arbitration). While bridge/memory controller 322 may be considered as a PCI bus master, any of the external devices coupled to PCI bus 334 may also act as a bus master." (Column 4, Lines 30-38)

The Applicants respectfully submit that neither of the references even if appropriately combined teach or suggest a programmable chip that includes both a memory controller and a processor. Neither of the references even if appropriately combined teach or suggest "wherein the memory controller is user configurable to either use separate sets of I/O lines for accessing off-chip tristate devices or to share one or more I/O lines for accessing off-chip tristate devices." Furthermore, Floman actually teaches away from such a combination.

The Examiner argues that Yip teaches in Figure 3 a programmable chip that includes both a memory controller and a processor. The Applicants respectfully disagree. Figure 3 shows a computer system, not a programmable chip. "Computer system 300 comprises a host processor system chip set which includes host processor 302, cache memory 304, bridge/memory controller 322, and dynamic random access memory 316. Host processor 302 may be any one of a number of commercially available microprocessors such as those marketed by Intel™ (Santa Clara, Calif.) and Motorola™ (Schaumburg, Ill.)." Commercially available microprocessors by Intel™ and Motorola™ are not processor cores that are included on a chip with a memory controller.

Furthermore, neither Yip nor Floman teach or suggest a memory controller that is "user configurable to either use separate sets of I/O lines for accessing off-chip tristate devices or to share one or more I/O lines for accessing off-chip tristate devices." In fact, neither Yip nor Floman even teach a memory controller that is user configurable.

The Examiner may attempt to argue, as the Examiner alludes to in the rejection to claim 5, that configuring hardware is well known. The Examiner takes official notice in the rejection to claim 5 that hardware is routinely configured under a graphical user interface such as Windows 95/XP using a registry or a control panel. It is acknowledged that it is possible to configure hardware using an interface such as Windows 95/XP. However, it is respectfully submitted that it is not well known and not obvious to provide a memory controller that is "is user configurable to either use separate sets of I/O lines for accessing off-chip tristate devices or to share one or more I/O lines for accessing off-chip tristate devices."

Furthermore, Floman actually teaches away from a combination suggested by the Examiner. Floman describes that a memory controller be an application specific integrated circuit (ASIC), which is a non user configurable device. Floman appears to suggest that the memory controller should not be user configurable.

Dependent claims 12 and 28 were rejected under 35 U.S.C. 103(a) as being unpatentable over Floman and Yip and further in view of Purcell (USP 6,836,815). The Examiner notes that Floman and Yip does not teach or suggest a simultaneous multiple primary component fabric. The Examiner argues that Purcell teaches this element. Purcell describes a multiple memory switch system. However, Purcell does not teach or suggest a simultaneous multiple primary component fabric. Although the processors in Purcell are able to access different memory banks through the multiple memory switch system, Purcell does not describe any instances where a primary component is accessing a secondary component while a separate primary component is accessing a separate secondary component. It is believed that Purcell only allows serial memory access to preserve cache coherency.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

Godfrey K. Kwan
Reg. No. 46,850

P.O. Box 70250
Oakland, CA 94612-0250
(510) 663-1100